SRI VENKATESWARA COLLEGE OF ENGINEERING
(AUTONOMOUS)
Karakambadi Road, Tirupati-517507

R 20

EXAMINATION BRANCH

M.Tech III Semester (R20) Regular & Supplementary Examinations February-2025
TIME TABLE

Exam Timings: **10.00 AM TO 1.00 PM**

Date/Day	VLSI Design (VLSI D)	Computer Science and Engineering (CSE)
04-02-2025 (Tuesday)	Bi-CMOS Technology and Applications EC20DPE301	Mobile Applications and Services CS20DPE301
	Optimization Techniques and Applications in VLSI Design EC20DPE302	High Performance Computing CS20DPE302
	System on Chip Architecture EC20DPE303	Optimization Techniques CS20DPE303
06-02-2025 (Thursday)	Business Analytics EC20DOE304	Quantum Computing CS20DOE304
	Composite Materials EC20DOE305	Industrial IOT CS20DOE305
	Industrial Safety EC20DOE306	Cyber Security CS20DOE306

Note: Any discrepancy in this time table may be brought to the notice of the under signed immediately.

COE
Date: 20-01-2025

Dy Chief Superintendent

Principal